PC-686(CPCI)-LV

CompactPCI Single Board Computer

For socket 370 CPU (Celeron™, Pentium III™)

With LAN/VGA

User's Manual

CONTEC

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Caution about Battery

Danger of explosion if battery is incorrectly replaced.

Replace only with the same or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer’s instructions.

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Chapter 1 Introduction

1.1 Specification

- **Processor Socket:** Socket 370
- **Processor:** Intel® Celeron™ 300MHz – 566MHz; Pentium III™ (FSB:100MHz) 500MHz – 700MHz
- **Host Bus:** CompactPCI Bus
  for PICMG2.0 R2.1 Bus Master is supported till 4 Max.
- **Chipset:** Intel® 440BX
- **Cache Size:** 128KB L2 cache is integrated in the Celeron™ CPU

  256KB L2 cache is integrated in the Pentium III™ CPU
- **Memory: Up to 768MB SDRAM**
- **Memory Sockets: Three 168-pin DIMM sockets for SDRAM in 8MB,** 16MB, 32MB, 64MB, 128MB and 256MB configurations.
- **BIOS:** Award BIOS, PnP support

Flash EEPROM (256KB) for BIOS update

Power management

Frequency / Voltage control

- **Bus Speed: 66MHz/100MHz**
- **Super I/O: Winbond W83977TF chipset**
- **Parallel port: One high-speed parallel port, SPP/EPP/ECP mode**
- **Series Port: Two 16550 UART port, COM2 is RS-232C/RS-422/RS-485 configurable**
- **Enhanced IDE: One EIDE port, up to 2 IDE devices, support Ultra DMA 33**
- **FDD Interface: Two floppy drives (360KB, 720KB, 1.2MB, 1.44MB, 2.88MB, LS-120)**
- **USB Interface: One stack connector support 2 USB ports**
- **Watchdog Timer: Software programmable 16 levels, Reset or NMI (Jumper selectable)**

- **Hardware Monitor: Winbond W83781D**
- **IrDA: One 1x6 Pin-header**
- **Keyboard connector: PS/2 keyboard connector**
- **Mouse connector: PS/2 Mouse connector**
- **VGA Connector: C&T 69000 Controller, 15 pin D-type VGA Connector**
- **LCD: C&T 69000 Controller, 41pin VESA Connector (for OEM)**
- **LAN: Intel 82559 LAN controller, RJ-45 connector**
- **SSD: DIP socket supports DiskOnChip flash disks (2MB~144MB)**
- **RTC: battery backup by Lithium Battery (CR2032)**

The coin type Lithium battery specification is shown in table

Specification	CR2032
Nominal Voltage	3V
Nominal Capacity	220mAh
Nominal Weight	3.1g

1.2 Mechanical & Environmental

- **POWER CONSUMPTION**

(Pentium III 700MHz)
+5VDC @6.50A Max.
+12VDC @250mA Max.
+3.3VDC @4.00A Max.

(Celeron 566MHz)
+5VDC @4.50A Max.
+12VDC @250mA Max.
+3.3VDC @3.50A Max.

- **OPTERATING TEMPERATURE: 0 ~ 60ºC.**
- **STORAGE TEMPPERATURE: - 40 ~ 80ºC.**
- **HUMIDITY: 10% to 90%**

- **BOARD DIMENSION: 160mm(L) x 233.35mm(H) / 6.23inch x 9.19inch.**
- **BOARD WEIGHT: 500g**

1.3 Check List

Please check that your package is complete and contains the items below. If you discover damaged or missing items, please contact your dealer.

- **The PC-686(CPCI) Industrial CPU Board**
- **This User's Manual & Registration Card**
- **1 IDE 40pin Ribbon Cable**
- **1 Floppy Ribbon Cable**
- **Driver disks utilities(floppy)**
- **Jumper Short Pin:6pcs.**
- **1 5pin DIN to 6pin mini-DIN Cable**
- **LCD exchange Display Board (for OEM)**
- **Memory (optional)**

  168PIN DIMM PC100 SDRAM 32MB "PC-MSD32-100"
  168PIN DIMM PC100 SDRAM 64MB "PC-MSD64-100"
  168PIN DIMM PC100 SDRAM 128MB "PC-MSD128-100"
  168PIN DIMM PC100 SDRAM 256MB "PC-MSD256-100"
  168PIN DIMM PC100 SDRAM 64MB with ECC "PC-MSD64E-100"
  168PIN DIMM PC100 SDRAM 128MB with ECC "PC-MSD128E-100"
  168PIN DIMM PC100 SDRAM 256MB with ECC "PC-MSD256E-100"

1.4 Description

The PC-686(CPCI) is a CompactPCI standard Industrial CPU board based on Intel's 440BX chipset and is fully designed for harsh industrial environment. It features socket 370 compatible with Intel's processor. This board accommodates up to 768MB of SDRAM memory.

The PC-686(CPCI) comes with onboard CPU temperature sensor to protect your processor from overheating (Winbond W83977HF chipset). Wired for Management (WFM) 2.0 specification compliance.

The PC-686(CPCI) has a LAN I/F that uses Intel 82559 PCI LAN controller.

The PC-686(CPCI) has a LCD Graphics that uses Chips 69000 graphic accelerator. The Chips 69000 features are show as following:

Integrated SDRAM Memory

- 2MB integrated memory
- 83 MHz SDRAM operation

Low Power Consumption

- 650mw

HiQColor™ Technology

The 69000 uses CHIPS proprietary TMED™ algorithm STN displays to produce:

- 256 Gray Shades
- 16.7M Colors
- Reduced motion artifacts
- Brighter cris per display.

Graphics Acceleration

- 64-bit Single Cycle BitBLT engine
- System/Screen-Screen BitBLT
- 256 3-op Raster Operations
- Color Expansion
- Instant Full Screen Page Flip

Simultaneous Hardware Cursor and Pop-up Window

- 64x64 pixels by 4 colors
- 128x128 pixels by 2 colors

Standards Supported

- Fully IBM® VGA Compatible
- ACPI
- VESA DPMS and DDC 1/2

Flexible Panel Support

- TFT, DSTN
- Color and Monochrome
- VGA, SVGA, XGA
- Auto Panel Power On/Off Sequencing

Multimedia video Acceleration

- Zoomed Video Port
- YUV/RGB data capture from video port or host bus
- Color Space Conversion (YUV-RGB)
- Horizontal and vertical interpolation
- Double Buffering
- Hardware Interrupt Support for VPE
- Color Key for Video Overlay
- Interlace/FRAME/Bob video capture

Integrated Clock Synthesizers

- 135 MHz RAMDAC
- 83 MHz Memory Clock with PLL

Advanced On-chip Power Management

- Standby mode
- Panel-off power saving mode
- Zero volt suspend
- Eight GPIO pins
- Activity Detection Output Pin

C&T 69000 Graphic Accelerator Refresh Rates

Resolution	Color	60(Hz)	75(Hz)	85(Hz)
640x480	8bbp	O	O	O
	16bbp	O	O	O
	24bbp	O	O	O
800x600	8bbp	O	O	O
	16bbp	O	O	O
	24bbp	O	O	O
1024x768	8bbp	O	O	O
	16bbp	O	O	O
1280x1024	8bbp	O	O	---

1.5 Power Management Features

1.5.1. Overview

The PIIX4 power management function provides a wide range of capabilities and configuration options allowing a system designer to implement a wide range of power saving modes.

PIIX4 provides for four main areas of power management:

- Clock Control and Processor Complex Management
- Peripheral Device Management
- System Management (SMI Generation, System Management Bus)
- System Suspend and Resume

Brief descriptions of primary power management function follow.

Clock Control: When the operating system, application program, or system software is not performing useful work, the processor complex (Processor, Host Bridge, DRAM, L2 cache) does not need to be executing cycles and, therefore, can be placed in Standby mode.

Peripheral Device Management: Peripheral device resources are monitored to detect when a specific device is idle. PIIX4 then informs system power management software, which can place that individual device into a power managed condition (such as Local Standby or Powered Off). Accesses targeting that device are then monitored.

System Suspend: Once the power management software has determined that the system is fully idle or that a critical system event has occurred, it can place the system into a suspend state, which allows for increased power savings. The software configured PIIX4 for the types of suspend, types of resume or wake-up events, and the PIIX4 automatically transitions the system into suspend. When an enabled resume event is detected, PIIX4 automatically restores the system operation.

- Three suspend states

- Power-on-Suspend (POS) with three system reset options
- Suspend-to-RAM (STR)
- Suspend-to-Disk (STD) or Soft OFF (SOff)

- Global Standby Timer (also active during suspend) to monitor for overall system idleness and as a resume timer
- Power Button Input
  - Override feature forcing immediate transition to Soft Off
- Battery Low indication pin
- Shadow registers for standard AT write only registers to save and restore system state information
- "Resume Well" to monitor wake-up events during suspend
- Resume power and reset sequencing

1.6 Power Requirements

Your system requires a clean, steady power source for reliable performance of the high frequency CPU on the PC-686(CPCI) Industrial CPU board, the quality of the power supply is even more important. For the best performance make sure your power supply provides a range of the following table DC power source.

1.6.1. Power Consumption

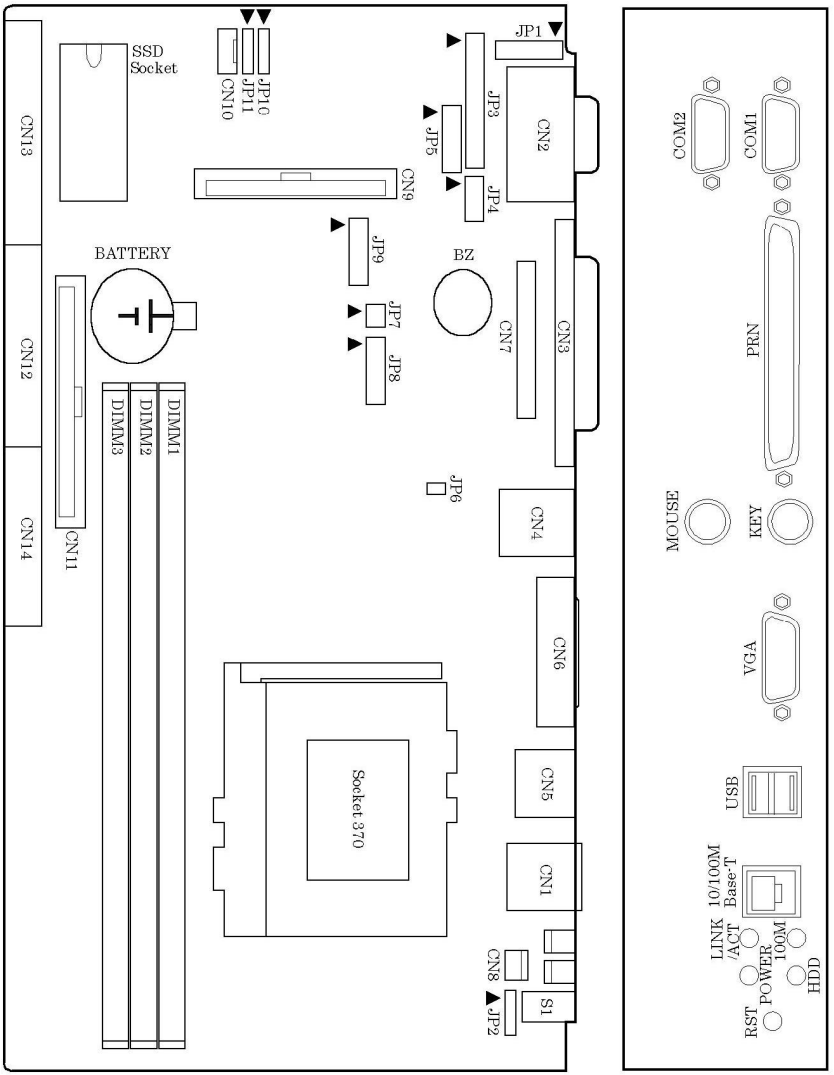
For typical configurations, the CPU board is designed to operate with at least a 200W power supply. A higher-wattage power supply should be used for heavily-loaded configurations. The power supply must meet the following requirements:

- Rise time for power supply: 2ms to 20ms
- Minimum delay for reset to Power Good: 100ms
- Minimum Powerdown warning: 1ms
- 3.3V output must reach its minimum regulation level within 20ms of the +5V output reaching its minimum regulation level

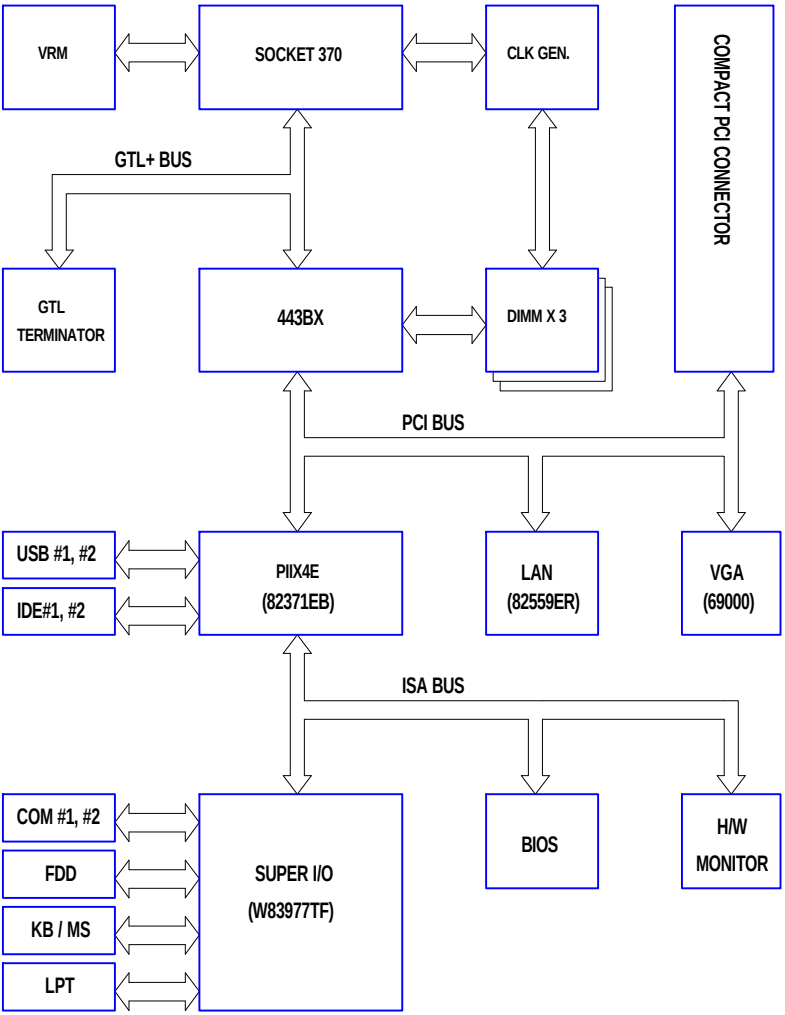
The following table lists the power supply's tolerances for DC voltages:

DC Voltage	*Acceptable Tolerance*
+3.3 V	± 4 %
+5 V	± 5 %
+12 V	± 5 %

1.7 Connector & Jumper Location



1.8 Block Diagram



Chapter 2 Hardware Installations

This chapter provides information on how to use the jumpers and connectors on the PC-686(CPCI) in order to set up a workable system.

2.1 Installation procedure

2.1.1 Install the processor with correct orientation.

2.1.2 Insert the DRAM module with correct orientation.

2.1.3 Mount the Fan on the top of the processor and connect it to FAN connector.

2.1.4 Insert all external cables except for flat panel. (Hard disk, floppy, keyboard, Mouse, LAN, etc.)

2.1.5 Prepare a CRT monitor for CMOS setup.

2.1.6 Confirm the power supply of Backplane is off.

2.1.7 Insert the CPU board to Backplane.

2.1.8 Turn on the power.

2.1.9 Enter the BIOS setup mode by pressing 'Del' key during boot up.

2.1.10 Use the "Load BIOS Optimal Defaults" feature.

2.1.11 Configure the ***Peripheral Setup*** and the ***Standard Setup*** correctly.

Note: *The CMOS memory may be in an undefined state at power-on after a period of no battery backup.*

2.2 CPU Installation:

The PC-686(CPCI) Industrial CPU Board supports **Intel® Celeron™ or Pentium III™ processor**. The processor's VID pins automatically program the Core voltage regulator on the CPU board to the required processor voltage. The host bus speed is automatically selected. The processor connects to the CPU board through the 370-pins ZIF PPGA socket.

The CPU board supports the processors listed in table below:

Processor	Processor Speed	Host Bus frequency	Cache size
Celeron	566MHz	66MHz	128KB
Pentium III	600MHz	100MHz	256KB
	700MHz	100MHz	256KB

The ZIF PPGA socket comes with a lever to secure the processor. Make sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket.

After you have installed the processor into the socket 370, check if the configuration setup for the CPU type and speed are correct. The CPU should always have a Heat Sink or Heat Sink with a cooling fan attached to prevent overheating.

Note: *Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

2.3 Main Memory Installation: DIMM1, DIMM2, DIMM3

The PC-686(CPCI) Industrial CPU Board supports three dual inline memory module (DIMM 168-pin) sockets for a maximum total memory of 768MB. Using the serial presence detect (SPD) data structure, programmed into an E^2PROM on the DIMM, the BIOS can determine the SDRAM's size and speed. Minimum memory size is 8MB; maximum memory size is 768MB. Memory size and speed can vary between sockets.

The CPU board supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 100 MHz SDRAM
- Non-ECC (64-bit) and ECC (72-bit) memory
- 3.3V memory only
- Unbuffered single or double-sided DIMMs in the following sizes:

2.3.1. SDRAM

SYNCHRONOUS DRAM (SDRAM) improves memory performance through memory access that is synchronous with the memory clock. Burst transfer rates at x-1-1-1 timing can be achieved using SDRAM, while asynchronous memory subsystems are typically limited at x-2-2-2 transfer rates.

The CPU board supports single or double-sided DIMMs in the following sizes:

DIMM size	Non-ECC configuration	ECC configuration
16MB	2Mbit x 64	2Mbit x 72
32MB	4Mbit x 64	4Mbit x 72

DIMM size	Non-ECC configuration	ECC configuration
64MB	8Mbit x 64	8Mbit x 72
128MB	16Mbit x 64	16Mbit x 72
256MB	32Mbit x 64	32Mbit x 72

Note: *All memory components and DIMMs used with the PC-686(CPCI) CPU board must comply with the PC SDRAM Specification. These include: the PC SDRAM Specification *memory component specific), the PC Unbuffered DIMM Specification, and the PC Serial Presence Detect Specification.*

2.3.2. Chipset

The Intel 441BX PCIset includes a Host-PCI bridge integrated with both an optimized DRAM controller and an A.G.P. Interface. The I/O subsystem of the 440BX is based on the PIIX4E, which is a highly integrated PCI-ISA/IDE Accelerator Bridge. This chipset consists of the Intel 82443BX PCI/A.G.P. controller (PZC) and the Intel 82371EB PCI/ISA IDE Xccelerator (PIIX4E) bridge chip.

Intel 82443BX PCI/A.G.P. Controller (PAC)

The PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the A.G.P., and main memory. The PAC features:

- Processor Interface control
  - Support for processor host bus frequencies of 100MHz or 66 MHz
  - 32-bit addressing
  - desktop Optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for:
  - +3.3V only DIMM DRAM configurations
  - Up to three double sided DIMMs

- 100-MHz SDRAM
- DIMM serial presence detect via SMBus interface
- 16 and 64-Mbit devices with 2K, 4K and 8K page sizes
- x4, x8, x16, and x32 DRAM widths
- SDRAM 64-bit data interface with ECC support
- Symmetrical and asymmetrical DRAM addressing

- A.G.P. interface
  - Complies with the A.G.P. specification
  - Support for +3.3V A.G.P. 66/133 devices
  -

  Synchronous coupling to the host-bus frequency

- PCI bus interface
  - Complies with the PCI specification
  - Asynchronous coupling to the host-bus frequency
  - PCI parity generation support
  - Data streaming support from PCI-to-DRAM
  - Support for five PCI bus masters in addition to the host and PCI-to-ISA I/O bridge
  - Support for concurrent host, A.G.P., and PCI transactions to main memory

- Data buffering
  - DRAM write buffer with read-around-write capability
  - Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1-to-DRAM read

buffers

- A.G.P. dedicated inbound/outbound FIFOs (133/66 MHz), used for temporary data storage

- Power management functions
  - Support for system suspend/resume (DRAM and power-on suspend)
  - Compliant with ACPI power management
- SMBus support for desktop management functions
- Support for system management mode (SMM)

Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E)

The PIIX4E is a multifunction PCI device implementing the PCI-to-ISA bridge, PCI IDE functionality, USB host/hub functionality, and enhanced power management. The PIIX4E features:

- Multifunction PCI-to-ISA bridge
  - Support for the PCI bus at 33MHz
  - Complies with the PCI specification
  - Full ISA bus support
- USB controller
  - Two USB ports
  - Support for legacy keyboard and mouse
  - Support for UHCI interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16MB/sec
  - Support for Ultra DMA/33 synchronous DMA mode transfers up to

33MB/sec

- Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfer

- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Support for PCI DMA with three PC/PCI channels and distributed DMA protocols
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
- Real-time Clock
  - 256-byte battery-backed CMOS SRAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54

Accelerated Graphics Port (A.G.P.)

A.G.P. is a high-performance bus for graphics-intensive applications, such as 3D applications. A. G. P., while based on the PCI Local Bus Specification, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. A. G. P. overcomes certain limitations of the PCI bus related to handling a large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency

- Demultiplexing of address and data on the bus for near 100 percent bus efficiency

- AC timing for 133MHz data transfer rates, allowing real data throughput in excess of 500 MB/sec

2.4 RJ-45 LAN connector: CN1

The PC-686(CPCI) CPU board is used Intel® 82559 PCI LAN chipset for LAN controller, the controller's features include:

- CSMA/CD Protocol Engine

- PCI bus interface

- DMA engine for movement of commands, status, and network data across PCI bus

- Integrated physical layer interface, including:

  1. Complete functionality necessary for the 10Base-T and 100Base-TX network interfaces; when in 10Mbit/sec mode, the interface drives the cable directly

  2. A complete set of Media Independent Interface (MII) management registers for control and status reporting

  3. 802.3u Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices, whether half- or full-duplex capable

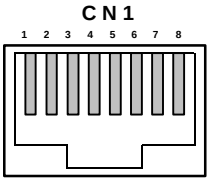
- Integrated power management features, including:

  1. Support for APM

This connector is for the 10/100Mbps Ethernet capability of the CPU board.

The follow table shows the pin assignments of this connector.

- The category-5 cable is required for transmission at 100Mbps.

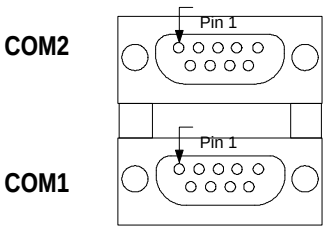


PIN No.	Function
1	TX+
2	TX-
3	RX+
4	N.C.
5	N.C.
6	RX-
7	N.C.
8	N.C.

2.5 Serial Port connector: CN2

COM1 and COM2 is a connector that with two 9 pin D-type header, is onboard serial ports of the CPU board PC-686(CPCI). The following table shows the pin assignments of these connectors.

RS-422/RS-485 assigned for COM2 connector only



PIN	RS-232C	RS-422	RS-485
1	DCD	TX-	TX-
2	RXD	TX+	TX+
3	TSD	RX+	RX+
4	DTR	RX-	RX-
5	GND	GND	GND
6	DST	RTS-	N.C.
7	RTS	RTS+	N.C.
8	CTS	CTS+	N.C.
9	RI	CTS-	N.C.

Note:

- *For RS-485, TX+(pin 2) and RX+ (pin 3) must jumper together inside the D type connector.*
- *TX- (pin 1) and RX- (pin 4) is the same.*

2.5.1. RS-422/RS-485 specifications

- Transmission system: Asynchronous, half-/full-duplex serial transmission conforming to RS-422/RS-485
- Baud rate: 19200 to 50bpx (programmable)
- Signal extensible distance: 1.2km Max.

Note: *The mouse and keyboard can be plugged into either PS/2 connector. Power to should be turned off before a keyboard or mouse is connected or disconnected.*

The keyboard controller contains code, which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del>, software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power On Self Test (POST).

Infrared Support

On the front panel I/O connector, there are six pins that support Hewlett Packard HSDL-1000 compatible infrared (IR) transmitters and receivers. In the Setup program, Serial Port B can be directed to a connected IR device. (In this case, the serial Port B connector cannot be used.) The IR connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbit/sec at a distance of 1 meter.

Consumer Infrared Support

On the front panel I/O connector, there is one pin that supports consumer infrared devices (remote controls). This pin supports receive-only operations at data rates of up to 685.57 Kbit/sec.

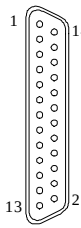
Consumer infrared devices can be used to control telephony and multimedia operations, such as volume or CD track changes. A software and hardware interface is needed for a computer to support the consumer infrared feature.

2.6 Parallel Port Connector: CN3

The parallel port bracket can used to add an additional parallel port for additional parallel devices. There are four options for parallel port operation:

- Compatible (Standard mode)
- Bi-Directional (PS/2 compatible)
- Bi-Directional EPP. A driver from the peripheral manufacturer is required for operation.
- Bi-Directional High-speed ECP

CN3



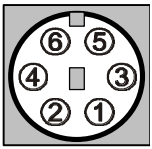
PIN No.	Function	PIN No.	Function
1	STROBE	14	ALF
2	PD0	15	ERROR
3	PD1	16	INIT
4	PD2	17	SLCT IN
5	PD3	18	GND
6	PD4	19	GND
7	PD5	20	GND
8	PD6	21	GND
9	PD7	22	GND
10	ACK	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

2.7 PS/2 Mouse & Keyboard stack Connector: CN4

The CPU board provides a standard PS/2® mouse mini DIN connector for attaching a PS/2® mouse. You can plug a PS/2® mouse directly into this connector. The Connector pin definition is shown below:

Mouse

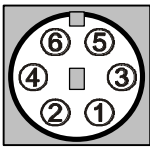
CN4



PIN No.	Function
1	Mouse DATA
2	N.C.
3	GND
4	+5V
5	Mouse CLOCK
6	N.C.

Keyboard

CN4



PIN No.	Function
1	K.B DATA
2	N.C.
3	GND
4	+5V
5	K.B CLOCK
6	N.C.

2.8 USB Connector: CN5

The Universal Serial Bus (USB) that allows plug and play computer peripherals such as keyboard, mouse, joystick, scanner, printer, modem/ISDN, CD-ROM and floppy disk drive to be automatically detected when they are attached physically without having to install drivers or reboot.

The USB connectors allow any of several USB devices to be attached to the computer. Typically, the device driver for USB devices is managed by the operating system. However, because keyboard and mouse support may be needed in the Setup program before the operating system boots, the BIOS supports USB keyboards and mice.

The CPU board has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel connectors. The CPU board fully supports the universal host controller interface (UHCI) and uses UHCI-compatible software drivers.

USB features includes:

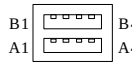
- Self-identifying peripherals that can be plugged in while the computer is running (USB Ver1.1)
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

Note: *Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*

This board has USB I/F 2ch.

It is a USB connector. The pin assignments are as follows:

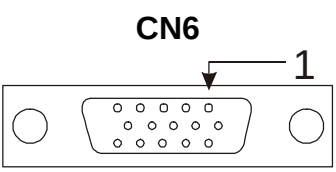
CN5



Pin No.	Signal name	Pin No.	Signal name
A2	USB0 Vcc	B1	USB1 Vcc
A3	USB0 –Data	B2	USB1 –Data
A4	USB0 +Data	B3	USB1 +Data
	USB0 GND	B4	USB1 GND

2.9 VGA Connector: CN6

It is a VGA CRT connector (HD-SUB15[Female]).
The pin assignments are as follows:

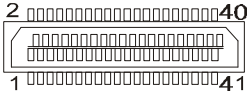


PIN No.	Function	PIN No.	Function
1	RED	**9**	N.C.
2	GREEN	**10**	GND
3	BLUE	**11**	D-DATE
4	N.C.	**12**	N.C.
5	GND	**13**	H-SYNC
6	GND	**14**	V-SYNC
7	GND	**15**	D-DCLK
8	GND		

2.10 LCD Connector: CN7

CN7 is a 41-pin connector for flat panel LCD displays. The following shows the pin assignments of this connector.(HIROSE DF9A-41P-1V)

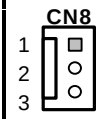
When you use the LCD display series(CONTEC products), you need the LCD exchange display board (for OEM).



PIN No.	Function	PIN No.	Function
1	DP20	**2**	GND
3	DP16	**4**	VCC
5	DP21	**6**	DP0
7	DP17	**8**	DP8
9	DP22	**10**	DP1
11	DP18	**12**	DP9
13	DP23	**14**	DP2
15	DP19	**16**	DP10
17	VCC	**18**	DP3
19	FLM	**20**	DP11
21	MX	**22**	DP4
23	LP	**24**	DP12
25	SHFCLK	**26**	DP5
27	3.3V	**28**	DP13
29	3.3V	**30**	DP6
31	ENABLK	**32**	DP14
33	LCDVDD	**34**	DP7
35	ENVEE	**36**	DP15
37	GND	**38**	+12V
39	GND	**40**	+12V
41	N.C.		

2.11 CPU FAN Connector: CN8

CN8 is a 3-pins box-header for the CPU cooling fan power connector. The fan must be a 12V fan. Pin 3 is for Fan speed sensor input.



PIN No.	Function	Housing:5102-03(Molex)
1	GND	Contact:5103(Molex)
2	DC+12V	
3	FAN_Sensor	

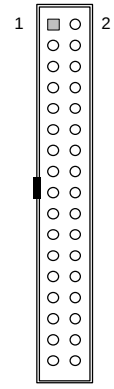
2.12 Floppy Disk Connector: CN9

In the Setup program, the floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

This connector supports the provided floppy drive ribbon cable. After connecting the single and to the board, connect the two plugs on the other end to the floppy drives.

CN9



PIN No.	Function	PIN No.	Function
1	GND	**2**	RWC
3	GND	**4**	N.C.
5	GND	**6**	N.C.
7	GND	**8**	INDEX
9	GND	**10**	DS0
11	GND	**12**	DS1
13	GND	**14**	DS2
15	GND	**16**	MOT ON
17	GND	**18**	DIR
19	GND	**20**	STEP
21	GND	**22**	WD
23	GND	**24**	WG
25	GND	**26**	TRCK 0
27	GND	**28**	WP
29	GND	**30**	RD
31	GND	**32**	SIDE 1
33	GND	**34**	DSK CHG

2.13 External Battery Connector: CN10

It is a 2 Pin connector used for external battery. An external battery powers the real-time clock and CMOS memory.

CN10	PIN No.	Function	Housing:XHP-2(JST)
	1	GND	Contact:SXH-001T-P0.6(JST)
	2	Ext_bat	

Note: *In using the external battery, you need 1-2pin short of JP11. And the available external battery is Lithium battery that the Voltage is 3V.*

2.14 Primary IDE port Connector: CN11

The CPU board PC-686(CPCI) has one independent bus-mastering PCI IDE interface. This interface support PIO Mode 3, PIO Mode 4, ATAPI devices (e.g., CD-ROM), and Ultra DMA/33 synchronous-DMA mode transfers. The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The BIOS automatically detects the IDE device transfer rate and translation mode.

Programmed I/O operations usually require a substantial amount of processor bandwidth. However, in multitasking operating systems, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

The CPU board PC-686(CPCI) also supports laser servo (LS-120) technology allows the user to perform read/write operations to LS-120 (120 MB) and conventional 1.44 MB and 720 KB diskettes. An optical server system is used to precisely position a dual-gap head to access the diskette's 2,490 tracks per inch (tpi) containing up to 120MB of data storage. A conventional diskette uses 130 tpi for 1.44MB of data storage.

LS-120 drives are ATAPI-compatible and connect to the CPU board's IDE interface. (LS-120 drives are also available with SCSI and parallel port interfaces.) Some versions of Windows 95 and Windows NT operating system recognize the

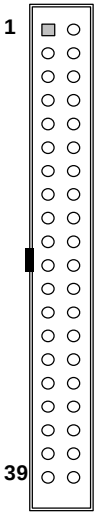
LS-120 drive as a bootable device in both 120 MB and 1.44MB mode.

Connection of an LS-120 drive and a standard 3.5-inch diskette drive is allowed. The LS-120 drive can be configured as a boot device if selected as Drive A in the BIOS setup program.

Note: *If you connect an LS-120 drive to an IDE connector and configure it as "boot" drive and configure a standard 3.5-inch diskette drive as a "B" drive, the standard diskette drive is not seen by the operating system. When the LS-120 drive is configured as the "boot" device, the system will recognize it as both the A and B drive.*

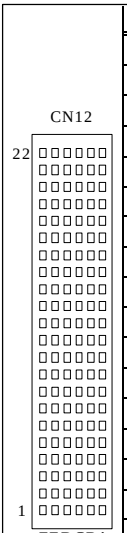
These connectors support the provided IDE hard disk ribbon cable. After connecting the single end to the board, connect the two plugs at the other end to your hard disk(s). If you install two hard disks, you must configure the second drive to Slave mode by setting its jumper accordingly. Please refer to your hard disk documentation for the jumper setting.

CN11



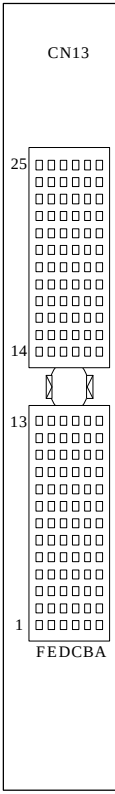
PIN No.	Function	PIN No.	Function
1	RESET	**2**	GND
3	D7	**4**	D8
5	D6	**6**	D9
7	D5	**8**	D10
9	D4	**10**	D11
11	D3	**12**	D12
13	D2	**14**	D13
15	D1	**16**	D14
17	D0	**18**	D15
19	GND	**20**	N.C.
21	DREQ	**22**	GND
23	IOW	**24**	GND
25	IOR	**26**	GND
27	IORDY	**28**	ALE
29	DACK	**30**	GND
31	IRQ	**32**	IOCS16
33	A1	**34**	PDIAG
35	A0	**36**	A2
37	CS0	**38**	CS1
39	HD ACT	**40**	GND

2.15 CompactPCI connector P2: CN12



Pin No.	A	B	C	D	E	E
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
4	VIO	BRSVP2B4	C-BE7#	GND	C/BE6#	GND
5	C/BE5#	GND	VIO	C/BE4#	PAR64	GND
6	AD63	AD62	AD61	GND	AD60	GND
7	AD59	GND	VIO	AD58	AD57	GND
8	AD56	AD55	AD54	GND	AD53	GND
9	AD52	GND	VIO	AD51	AD50	GND
10	AD49	AD48	AD47	GND	AD46	GND
11	AD45	GND	VIO	AD44	AD43	GND
12	AD42	AD41	AD40	GND	AD39	GND
13	AD38	GND	VIO	AD37	AD36	GND
14	AD35	AD34	AD33	GND	AD32	GND
15	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
16	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
17	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
18	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
19	GND	GND	N.C.	N.C.	RSV	GND
20	CLK5	GND	N.C.	GND	RSV	GND
21	CLK6	GND	N.C.	N.C.	RSV	GND
22	GA4	GA3	GA40	GA1	GA0	GND

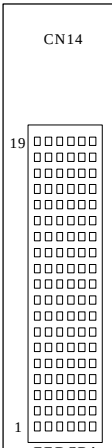
2.16 CompactPCI connector P1: CN13



Pin No.	A	B	C	D	E	F
1	VCC	–12V	TRST#	+12V	VCC	GND
2	TCK	VCC	TMS	TDO	TDI	GND
3	INTA#	INTB#	INTC#	VCC	INTD#	GND
4	BRSVP1A	GND	VIO	INTP	INTS	GND
5	BRSVP1A	BRSVP1B	RST#	GND	GNT#	GND
6	REQ#	GND	3.3V	CLK	AD31	GND
7	AD30	AD29	AD28	GND	AD27	GND
8	AD26	GND	VIO	AD25	AD24	GND
9	C/BE3#	IDSEL	AD23	GND	AD22	GND
10	AD21	GND	3.3V	AD20	AD19	GND
11	AD18	AD17	AD16	GND	C/BE2#	GND
12	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
13	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
14	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
16	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
17	3.3V	SDONE	SBO#	GND	PERR#	GND
18	SERR#	GND	3.3V	PAR	C/BE1#	GND
19	3.3V	AD15	AD14	GND	AD13	GND
20	AD12	GND	VIO	AD11	AD10	GND
21	3.3V	AD9	AD8	M66EN	C/BE0#	GND
22	AD7	GND	3.3V	AD6	AD5	GND
23	3.3V	AD4	AD3	VCC	AD2	GND
24	AD1	VCC	VIO	AD0	ACK64#	GND
25	VCC	REQ64#	ENUM#	3.3V	VCC	GND

2.17 CompactPCI connector P3: CN14

This Connector is connected to IDE Connector Signal and Floppy Disk Connector Signal.

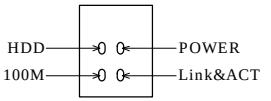


Pin No.	A	B	C	D	E	F	
1	DSKCHG#	HEAD#	WRATA#	WPRT#	N.C.	GND	Floopy Signals
2	TRAK0#	WGATE#	WDATA#	STEP#	N.C.	GND	
3	FDIR#	MOTB#	DSA#	DSB#	N.C.	GND	
4	MOTA#	INDEX#	DS1#	RWC#	N.C.	GND	
5	N.C.	N.C.	N.C.	N.C.	N.C.	GND	
6	FDCS#3	PDCS#1	PDA2	PDA0	IDEACT#	GND	IDE Primary Signals
7	PDA1	IPQ14	PDDACK3	PDIORDY	PDIAG	GND	
8	PDIOR#	PDIOW#	PDREQ	PDD15	N.C.	GND	
9	PDD0	PDD14	PDD1	PDD13	N.C.	GND	
10	PDD2	PDD12	PDD3	PDD11	N.C.	GND	
11	PDD4	PDD10	PDD5	PDD9	N.C.	GND	
12	PDD6	PDD8	PDD7	PDRST#	IDE ACT#	GND	
13	SDCS#3	SDCS#1	SDA2	SDA0	N.C.	GND	IDE Secondary Signals
14	SDA1	IRQ15	SDDACK#	SDIORDY	SDIAG	GND	
15	SDIOR#	SDIOW#	SDREQ	SDD15	N.C.	GND	
16	SDD0	SDD14	SDD1	SDD13	N.C.	GND	
17	SDD2	SDD12	SDD3	SDD11	N.C.	GND	
18	SDD4	SDD10	SDD5	SDD9	N.C.	GND	
19	SDD6	SDD8	SDD7	SDRST#	N.C.	GND	

2.18 Reset button: S1

When you press the button, then can reset your computer system.

2.19 LED Indicator

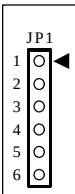


POWER	: POWER ON
HDD	: HDD SIGNAL
Link&ACT	: TX&RX
100M	: 100BASE-T

Chapter 3 Jumper Setting

3.1 Infrared (IrDA) port: JP1

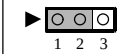
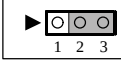
Serial Port 2 can be configured to support an IrDA module connected to this 6-pin header. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs and printers using application software. This connector is for optional wireless transmitting and receiving infrared module. You must configure the setting through the BIOS setup to use the IR function.



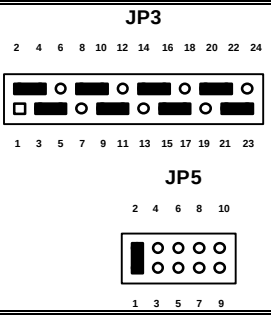
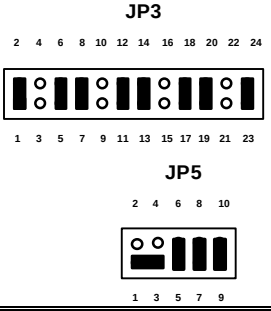
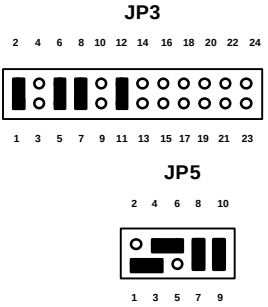
Pin No.	Function
1	IRTX
2	GND
3	IRRX
4	N.C.
5	5V
6	3.3V

3.2 Watchdog Timer output selector: JP2

When the watchdog timer activates, setup involves two jumpers. CPU processing has come to a halt, it can reset the system or generate a NMI. This can be setting JP11 as shown below:

JP2	Function
	NMI(Default)
	Reset

3.3 CN16 RS-232C/RS-422/RS-485 Selector: JP3/JP5

RS-232C (Default)	
RS-422	
RS-485	

1. For RS-485, TX+(pin 2) and RX+ (pin 3) must jumper together inside the D type connector.
2. TX- (pin 1) and RX- (pin 4) is the same.

3.3.1. Transmit date control in half-duplex mode

In half-duplex mode, the transmission buffer must be controlled to prevent transmit data from causing a collision. The PC-686(CPCI) uses the RTS signal and bit 1 in the modem control register to control transmit data.

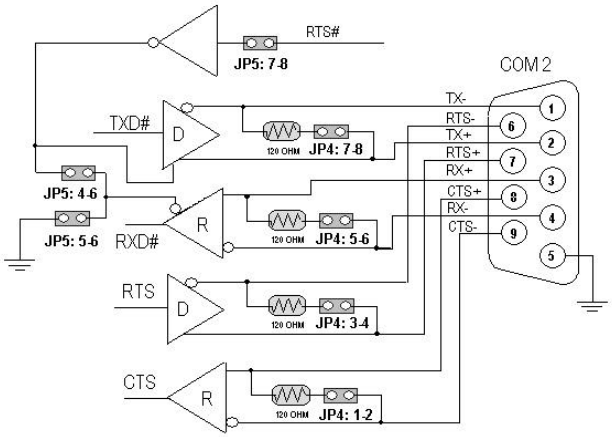
Modem control register

(Setting I/O address +4H) bit 1: 0 … RTS High (Disables transmission)
1 … RTS low (Enables transmission)

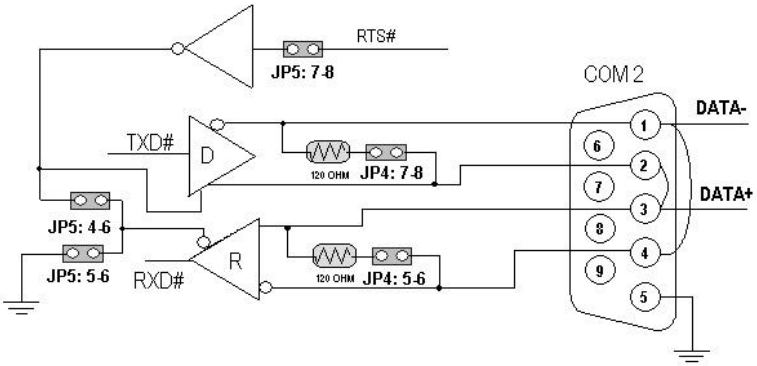
3.3.2. Setting the RS-422/RS-485 receiver disable control jumper

When the RS-422/RS-485 port is used, the RTS signal is used for driver enable control Connecting JP1 Pins 4 and 6 disables the receiver at the same time, preventing the port from receiving output data to an external device.

RS-422 Setting



RS-485 Setting



3.3.3. I/O addresses and instructions

The table below lists I/O addresses for use as COM2.

I/O address	DLAB	Read/Write	Register	
02F8H	0	W	Transmitter holding Register	THR
		R	Receiver buffer Register	RBR
	1	W	Divisor latch Register (LSB)	DLL
02F9H	1	W	Divisor latch Register (MSB)	DLM
	0	W	Interrupt enable Register	IER
02FAH	X	R	Interrupt ID Register	IIR
02FBH	X	W	Line control Register	LCR
02FCH	X	W	Modem Control Register	MCR
02FDH	X	R	Line status Register	LSR
02FEH	X	R	Modem Status Register	MSR
02FFH	X	R/W	Scratch Register	SCR

3.4 RS-422/RS-485 Terminator: JP4

JP4	Terminator	Function
	-	No terminating resister (Default)
	CTS for RS-422	terminating resister provided
	RTS for RS-422	terminating resister provided
	RXD for RS-422/RS-485	terminating resister provided
	TXD for RS-422/RS-485	terminating resister provided

3.5 On board LAN selector: JP6

JP6	Function
	Disabled
	Enabled (Default)

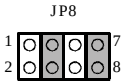
3.6 DISK ON CHIP Memory Add. Selector: JP7

You can select the memory address by JP7 setting, after equip DiskOnChip with the SSD Socket. Below are 4 kinds of DiskOnChip memory address configuration.

JP7	Function
JP7 	0DC00~ 0DDFFh
JP7 	0D800h~0D9FFh
JP7 	0D400h~0D5FFh
JP7 	0D000h~0D1FFh (Default)

3.7 Display Type Setting: JP8

In case of connecting LCD with CN7, it is corresponding to OEM. And generally please use on the no use LCD setting (below).



3.8 CPU frequency ration setting: JP9

This board will set the CPU frequency ration automatically. Default setting is all open. Keep JP9 all-open.

3.9 Clear CMOS Content: JP10

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program. The RAM data contains the password information is powered by the onboard button cell battery. User can erase the CMOS memory content by short pin2 and pin3 of JP10 together.

An external coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3V standby current from the power supply extends the life of the battery. The clock is accurate to ±2 minutes/month at 25ºC with 3.3V applied.

JP10	Function
JP10 1 2 3	Normal Operation (Default)
JP10 1 2 3	Clear CMOS Content

3.10 External/Internal battery selector: JP11

JP11	Function
JP11 1 2 3	Select to the external battery
JP11 1 2 3	Select to the internal battery (Default)

Note: *In using the external battery, please short 1-2pin of JP11.*

Chapter 4 CPU Board Resources

4.1. I/O MAP

Address (hex)	Size	Description
0000 ~ 000F	16 bytes	DMA Controller
0020 ~ 0021	2 bytes	Interrupt Control (PIC)
002E ~ 002F	2 bytes	Super I/O controller configuration registers
0040 ~ 0043	4 bytes	System timer 1
0048 ~ 004B	4 bytes	System timer 2
0060	1 byte	Keyboard Controller
0061	1 byte	NMI, speaker control
0064	1 byte	Keyboard controller
0070 ~ 0071	2 bytes	Real Time Clock Controller
0080 ~ 008F	16 bytes	DMA page registers
00A0 ~ 00A1	2 bytes	Interrupt controller 2
00B2 ~ 00B3	2 bytes	APM control
00C0 ~ 00DE	31 bytes	DMA controller 2
00F0 ~ 00FF	16 bytes	Numeric processor
0170 ~ 0177	8 bytes	Secondary IDE controller
01F0 ~ 01F7	8 bytes	Primary IDE controller
0228 ~ 022F*	8 bytes	LPT3
0274 ~ 0277	4 bytes	I/O read data port for ISA PnP enumerator
0278 ~ 027F*	8 bytes	LPT2
02E8 ~ 02EF*	8 bytes	COM4/Video (8514A)
02F8 ~ 02FF*	8 bytes	COM2
0376 ~ 0377	2 bytes	Secondary IDE channel
0295,0296	2 bytes	Hard Ware Monitor
0378 ~ 037F	8 bytes	LPT1

Address (hex)	Size	Description
03B0 ~ 03BB	12 bytes	Video (Monochrome)
03C0 ~ 03DF	32 bytes	Video (VGA)
03E8 ~ 03EF	8 bytes	COM3
03F0 ~ 03F5, 03F7	8 bytes	Diskette controller
03F6	1 byte	Primary IDE channel
03F8 ~ 03FF	8 bytes	COM1
04D0 ~ 04D1	2 bytes	Edge/level triggered PIC
LPT n + 400h	8 bytes	ECP port, LPT n base address + 400h
0CF8 ~ 0CFF**	4 bytes	PCI configuration address register
0CF9***	1 byte	Turbo and reset control register

** Dword access only
*** Byte access only

4.2. MEMORY MAP

Address Range (H)	Size	Description
100000-18000000	512MB	Extended memory
E8000-FFFFF	96KB	System BIOS
E0000-E7FFF	32KB	System BIOS (Available as UMB)
C8000-DFFFF	96KB	Available high DOS memory (open to ISA and PCI buses)
A0000-C7FFF	160KB	Video memory and BIOS
00000-9FFFF	640KB	Conventional memory

4.3. DMA Channels

DMA	Data Width	System Resources
0	8 or 16bits	Reserved
1	8 or 16bits	Reserved(or parallel port (for ECP))
2	8 or 16bits	Diskette drive
3	8 or 16bits	Reserved(or parallel port (for ECP))
4	---	Reserved – cascade channel
5	16bits	Open
6	16bits	Open
7	16bits	Open

4.4. PCI Configuration Space Map

Bus #	Device #	Function #	Description
00	00	00	Intel® 82443BX (PAC)
00	01	00	Intel® 82443BX PCI-to-PCI bridge (for A. G. P.)
00	07	00	Intel® 82371EB (PIIX4E) PCI/ISA bridge
00	07	01	Intel® 82371EB (PIIX4E) IDE bridge
00	07	02	Intel® 82371EB (PIIX4E) USB
00	07	03	Intel® 82371EB (PIIX4E) power management
00	0D	00	PCI expansion slot 1
00	0E	00	PCI expansion slot 2
00	0F	00	PCI expansion slot 3
00	10	00	PCI expansion slot 4
01	00	00	A. G. P. connector

4.5. Interrupters

IRQ #	System Resources
NMI	I/O Channel check
0	Reserved, interval timer
1	Reserved, keyboard controller
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option)/audio/user available
6	Diskette drive controller
7	LPT1*
8	Real time clock
9	ACPI
10	USB/User available
11	User available
12	PS/2 mouse port (if present, else user available) It need to set "Disabled" in BIOS.
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

4.6. PCI Interrupters Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in board.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in board that require only one interrupt are in this category. For almost all board that require more than one interrupt, the first interrupt on the board is also classified as INTA.
- INTB: Generally, the second interrupt on add-in board that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in board is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in board) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the CPU board and therefore share the same interrupt. The table below lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

PCI Interrupt Routing Map

PIIX4E PIRQ Signal	1st PCI Slot	2nd PCI Slot	3rd PCI Slot	4th PCI Slot	PCI Audio	A. G. P. Slot	USB	Power Management
PIRQA	INTA	INTD	INTC	INTB		INTA		INTA
PIRQB	INTB	INTA	INTD	INTC		INTB		
PIRQC	INTC	INTB	INTA	INTD	INTA			
PIRQD	INTD	INTC	INTB	INTA			INTA	

For example, assume an add-in board with one interrupt (Group INTA) into the fourth PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the onboard video and SB PCI sources. The add-in board shares an interrupt with these onboard interrupt sources.

Now however, plug and add-in board that has one interrupt (Group INTA) into the first PCI slot. Plug a second add-in board that has two interrupts (Group INTA and INTB) into the second PCI slot. INTA in the first slot is connected to signal PIRQA. INTA in the second slot is connected to signal PIRQB, and INTB is connected to signal PIRC. With no other boards added, the three interrupt sources on the first two boards each have a PIRQ signal to themselves. Typically, they will not share an interrupt.

Note: *The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.*

Chapter 5 Software Utilities

This chapter introduces the software utilities supplied for PC-686(CPCI) which including a 10/100M Ethernet driver, Intel® 440BX chipset Core PCI&ISAPNP services / Graphics drivers for CRT/Flat Panel Driver and watchdog function configuration utility.

5.1. Intel® 440BX chipset Driver

5.1.1. INF Installation Utility

System INF Utilities for Windows 98 Second Edition, Windows 98, Windows 95 OSR 2.x

The Intel® INF Installation Utility installs to the target system the INF files that outline to the operating system how the chipset components shall be configured. This is needed for proper functionality of the following features of the Intel® 440BX chipset.

Intel® INF Installation Utility for Windows 95 and Windows 98: setup.exe

One of the following operating systems must be installed on the system:

Windows 95 4.00.950 (Original Release)

Windows 95 4.00.950a (OSR1)

Windows 95 4.00.950b (OSR2 without USB Supplement)

Windows 95 4.00.950b (OSR2.1 with USB Supplement)

Windows 95 4.00.950c (OSR2.5 with or without USB Supplement)

Windows 98 4.10.1998 (Original Release)

Windows 98 Second Edition

4.10.2222 (Original Release)

5.2. Graphic Driver

5.2.1. Introduction

The CPU board PC-686(CPCI) is adopted the Chips 69000 for PCI board VGA / LCD designs.

The 69000 integrate high performance memory technology for the graphics frame buffer. Based on the proven HiQVideo™ graphics accelerator core, the 69000 combines state-of-the-art flat panel controller capabilities with low power, high performance integrated memory.

High Performance integrated Memory

The 69000 provide integrated high performance synchronous DRAM (SDRAM) that can support up to 83MHz for the graphics/video frame buffer. The bandwidth for the graphics subsystem. The result is support for additional high color / high-resolution graphics modes combined with real-time video acceleration.

Frame-Based AGP Compatibility

The 69000 graphics is designed to be used with either 33MHz PCI, or with AGP as a frame-based AGP device, allowing it to be used with the AGP interface provided by the latest core logic chipsets.

HiQColor™ Technology

The 69000 integrated CHIPS breakthrough HiQColor™ technology. Based on the CHIPS proprietary TMED (Temporal Modulated Energy Distribution) algorithm, HiQColor technology allows the display of 16.7 million true colors on STN panels without using Frame Rate Control (FRC) or dithering. Independent of panel response, the TMED algorithm eliminates all of the flaws (such as shimmer, Mach banding, and other motion artifacts) normally associated with dithering and FRC. Combined with the new fast response, high-contrast, and low-crosstalk technology found in new STN panels, HiQColor technology enables the best display quality and color fidelity previously only available with TFT technology.

Versatile Panel Support

The 69000 supports a wide variety of monochrome and color Single-panel, Single-Drive (SS) and Dual-Panel, Dual Drive (DD), standard and high-resolution, passive STN and active matrix TFT/MIM LCD, and EL panels. With HiQColor technology, up to 256 gray scales are supported on passive STN LCDs. Up to 16.7 different colors can be displayed on passive STN LCDs and up to 16.7M colors on 24 bit active matrix LCDs.

The 69000 offers a variety of programmable features to optimize display quality. Vertical centering and stretching are provided for handling modes with less than 480 lines on 480-line panels. Horizontal and vertical stretching capabilities are also available for both text and graphics modes for optimal display of VGA text and graphics modes on 800x600, 1024x768 and 1280x1024 panels.

HiQVidel Multimedia Support

The 69000 uses independent multimedia capture and display systems on-chip. The capture system places data in display memory and the display system places the data in a window on the screen.

The capture system can receive data from either the system bus or from the ZV enabled video port in either RGB or YUV format. The input data can also be scaled down before storage in display memory. Capture of input data may also be double buffered for smoothing and to prevent image tearing. To better support MPEG2 (DVD) video decompression, the 69000 includes a line buffer to directly support the native format of MPEG2 data of 720 pixels wide.

The capture engine also supports image mirroring and rotation for camera support. This feature is important for applications such as video teleconferencing because it allows the image movements to appear on the display as it actually occurs. The image and movement is not a mirror image of what is actually taking place.

The display system can independently place either RGB or YUV data from anywhere in display memory into an on-screen window which can be any size and located at any pixel boundary (YUV data is converted to RGB "on-the-fly" on

output). This is important for the 69000 since the video must be stored in the integrated 2MB frame buffer and thus optimized to require very little space. Storing data in the native YUV format uses less memory for video while providing excellent playback display quality.

Non-rectangular windows are supported via color keying. The data can be fractionally zoomed on output up to 8x to fit the on-screen window and can be horizontally and vertically interpolated. Interlaced and non-interlaced data are both supported in the capture and display systems.

Low Power Consumption

The 69000 uses a variety of advanced power management features to reduce power consumption of the display sub-system and to extend battery life. Optimized for 3.3V operation, the 69000 internal logic, bus and panel interfaces operate at 3.3V but can tolerate 5V operation.

Software Compatibility / Flexibility

The HiQVideo controllers are fully compatible with the VGA standard at both the register and BIOS levels.

CHIPS and third party vendors supply a fully VGA compatible BIOS, end-user utilities and drivers for common application programs.

Acceleration for All Panels and All Modes

The 69000 graphics engine is designed to support high performance graphics and video acceleration for all supported display resolutions, display types, and color modes. There is no compromise in performance operating in 8, 16, or 24bpp color modes allowing true acceleration while displaying up to 16.7M colors.

5.2.2. Driver Support

- Windows 95

  This driver allows CHIPS 69000 to support Windows 95. It is for the PCI Bus and supports DirectX 5 for the 69000:

- Windows NT 4.0, Windows NT 3.51

This driver allows Chips 69000 to support Windows NT 4.0.: ; Windows NT 3.51

- Windows 98

  This driver allows Chips 69000 to support Windows 98 platform: .

- Windows 3.1

  This driver allows CHIPS 69000 to support Windows 3.1:

- Windows 2000

  About Windows 2000, please use the standard VGA Drivers in the OS.

5.3. LAN Driver

5.3.1. Introduction

The CPU board PC-686(CPCI) is adopt 82559 10/100 Mbps Fast Ethernet controller with an integrated 10/100 Mbps for PCI board LAN designs.

5.3.2. Specifications

- Advanced Configuration and Power Interface (ACPI) 1.20A based power management
- Wake on Magic Packet
- Wake on interesting packet
- Advanced System Management Bus (SMB) based manageability
- Wired for Management (WFM) 2.0 compliance
- IP checksum assist
- PCI 2.2 compliance
- PC 98, PC 99, and Server 99 compliance.

LAN Drivers

- Windows 98, Windows 95 OSR2.x , Windows95 Retail,OSR1, Windows NT 4.0,NT3.51 : DISK1
- NDIS2.01 : DISK1
- NETWARE DOS ODI Client : DISK2
- NETWARE 3.12, 4.1x Server : DISK2

Note: *Before install the LAN utilities please refer to the files *.txt in the rootdirectory and subdirectory.*

5.4. Watchdog-Timer (WDT) Setting

WDT is widely used for industry application to monitoring the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. The WDT will not be reload by an abnormal system, then WDT will time out and reset the system automatically to avoid abnormal operation.

PC-686(CPCI) supports 16 levels watchdog timer by software programming I/O ports. Write any value to I/O address 0441H will disable Watch-Dog-Timer. Write setting code (please reference to WDT Setting Table) to I/O 0443h will re-load WDT.

Below is an assembly program example for disable and load of WDT.

```
MOV DX,0441H    REM Write any value to 0441H, disable WDT
OUT DX,AX;
MOV AX,0001H    REM set WDT timer = 28 Sec
MOV DX,0443H
OUT DX,AX    REM trigger WDT with timer setting
```

VALUE	TIMER	VALUE	TIMER	VALUE	TIMER	VALUE	TIMER
0	30 Sec.	4	22 Sec.	8	14 Sec.	C	6 Sec.
1	28 Sec.	5	20 Sec.	9	12 Sec.	D	4 Sec.
2	26 Sec.	6	18 Sec.	A	10 Sec.	E	2 Sec.
3	24 Sec.	7	16 Sec.	B	8 Sec.	F	0 Sec.

5.5. Update new version BIOS

Steps 1: Make a record of your original or existing BIOS Setup parameters. Press [Del] during the Power-On-Self-Test to enter BIOS Setup Program and write down the value of each parameter in order to re-configure your System after BIOS updating

Step 2: Make a System Disk. Put a 3.5 inch disk in Drive A. For MS-DOS, Key in "format a:/s" and press [Enter]. For Windows, select My Computer, click 3.5 inch Floppy (A:), select File/Format from Command Bar. On the "Format 3.5 inch Floppy (A:)" menu, select "Copy system files" and then click [Start] button.

Step 3: Copy the updated BIOS bin file and awdflash.exe file to the System Disk.

Step 4: Put the System Disk in Drive A and re-start your computer from Drive A.

Step 5: Begin to update your BIOS. Enter [awdflash] command, the "Flash Memory Writer" message will appear on screen. Enter the updated BIOS file name at "File Name to Program:". Enter the backup file name for the existing BIOS at "File Name to Save:". Press [Y] to proceed with the BIOS updating.

Step 6: Re-configure your system. Remove the System Disk and re-start your computer. Press [Del] during the Power-On-Self-Test to enter BIOS Setup Program. Re-set the relevant parameters according to your record of the Original setting. Save and Exit BIOS Setup program to re-boot your system.

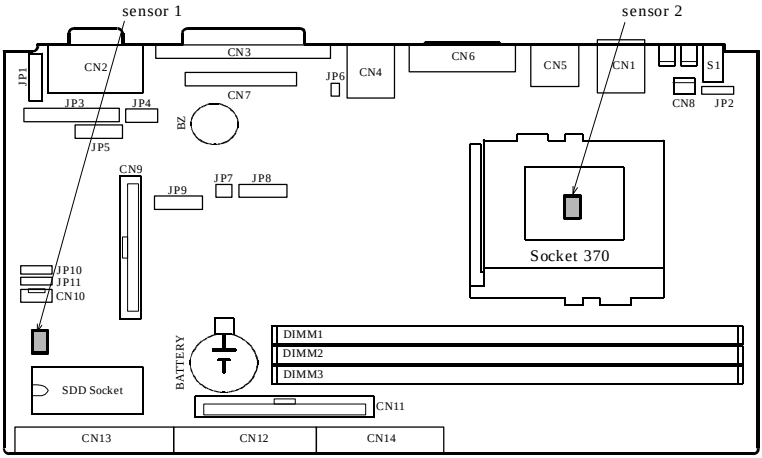
5.6. Hardware Monitor

Hardware Monitor function is included in Hardware Monitor controller (Winbond W83781D) on PC-686(CPCI)-LV.

You can read Temperature, Voltage and Fan Sensor output of SBC.

5.6.1. Temperature

Two Thermistors are mounted on SBC as following. You can read Temperature of this position.



5.6.2. Voltage

You can read 3.3V, +5V, -5V, +12V, -12V, VTT (1.5V), Vcore of SBC.

VTT(1.5V) : CPU I/O voltage
Vcore :CPU core voltage

5.6.3. Speed Sensor

FAN Speed Sensor signal is input in CN8 pin3 when you use FAN with speed sensor.

You can read FAN speed.
<Caution>

You mast use FAN with speed sensor if you would like to read FAN Speed.

5.6.4. W83781D Registers

There are two ports to read W83781D Hardware Monitor Registers.

These two ports are described as following.

Index Register : 295h
Data Register : 296h
The registers Index is showed as next page.

<Sample Program: Read Chip ID Register to bx>

```
mov ax, 4eh;
mov dx,295h;
out dx,ax;          (index register set for BANK select register)
inc dx;
out dx,80h;         (BANK=0 is set)
mov ax,58h;
mov dx,295h;
out dx,ax;          (index register set for Chip ID register)
inc dx;
in bx,dx;           (Read chip ID register to bx)
```

Hard Ware Monitor Register Index

Address	Auto-Increment Address	Description
20h	60h	Vcore reading
21h	61h	Vtt reading
22h	62h	+3.3V reading
23h	63h	+5V Reading
24h	64h	+12V Reading
25h	65h	-12V Reading
26h	66h	-5V Reading
27h	67h	Sensor Temperature reading
28h	68h	CN18 FAN sensor reading
29h	69h	Reserved
2Ah	6Ah	Reserved
2Bh-3Dh	6Bh-7Dh	Limit Registers (*1)
3Eh-3Fh	7Eh-7Fh	Reserved
40h-46h	-	Configuration registers (*1)
47h-49h	-	VID/Fan Register
48h-4Dh, 4Fh	-	Configuration registers (*1)
4Eh	-	50h-5Fh Bank Select register
BANK0		
50h	-	R-T Table index port (*1)
51h	-	R-T Table data port (*1)
52h-55h	-	Winbond Test register
56h-57h	-	Beep Control registers (*1)

58h	-	Chip ID Register <10h>
59h-5Fh	-	Reserved
BANK1		
50h-51h	-	Sensor 2 Temperature reading
52h-5Fh	-	Sensor2 Temperature Configuration Register (*1)
BANK2		
50h-5Fh	-	Sensor3 Temperature Register (not in use)
BANK3		
50h-5Fh	-	Reserved
BANK4		
50h-5Fh	-	Reserved
BANK5		
50h-5Fh	-	Reserved
BANK6		
50h-5Fh	-	Reserved

(*1) Please refer to W83781D manual in detail

Vcore reading Register(20h)

VTT(V) = 16mV x ReadData

VTT(1.5V) reading Register(21h)

Vcore(V) = 16mV x ReadData

+3.3V reading Register(22h)

V3.3(V) = 16mV x ReadData

+5V reading Register(23h)

V5(V) = 16mV x ReadData x 1.68

+12V reading Register(24h)

V+12(V) = 16mV x ReadData x 3.8

-12V reading Register(25h)

V-12(V) = (16mV x ReadData)- (3.48)

-5V reading Register(26h)

V-5(V) = ((16mV x ReadData)- (1.49)

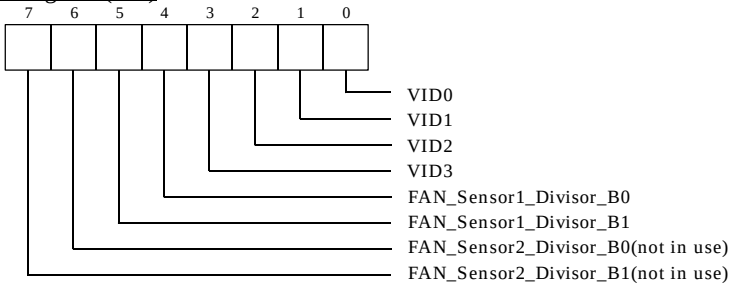
Temperature Sensor1 Temperature Register(27h)
Temperature Sensor1 Data Format Table:

Temperature	Temperature Sensor Register
+125ºC	7Dh
:	:
+25ºC	19h
:	:
+5ºC	05h
:	:
+1ºC	01h
+0ºC	00h
-1ºC	FFh
:	:
-5ºC	FBh
:	:
-25 ºC	E7h
:	:
-55 ºC	C9h

CN8 FAN sensor Reading Register(28h)

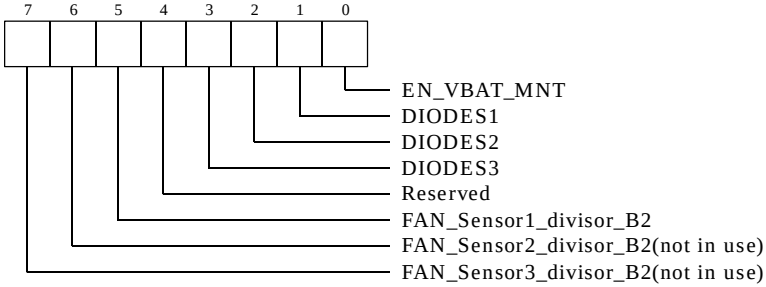
RPM = $1.35x10^6$ / (ReadData x FAN_sensor1_Divisor)

VID/FAN Register (47h)



Bit 7-6:FAN_Sensor2 Divisor Bit 1-0(not in use)
Bit 5-4:FAN_Sensor1 Divisor Bit 1-0
Bit 3-0:VID<3:0> Input

FAN Divisor Register (BANK0:5Dh)



Bit 7:FAN_Sensor3 Divisor Bit2(not in use)
Bit 6:FAN_Sensor2 Divisor Bit2(not in use)
Bit 5:FAN_Sensor1 Divisor Bit2
Bit 4:Reserved
Bit 3:Sensor 3 type selection(not in use)
Bit 2:Sensor 2 type selection(not in use)
Bit 1:Sensor 1 type selection (Set to "0")
Bit 0:Battery Monitor Enable/Disable (1:Enable,0:Disable)

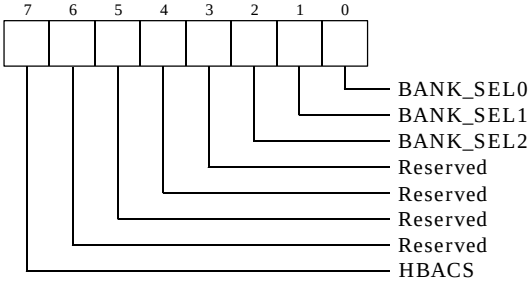
FAN Divisor Table:

Bit1	Bit0	Divisor
0	0	1
0	1	2
1	0	4
1	1	8

VID(Vcore) Table:

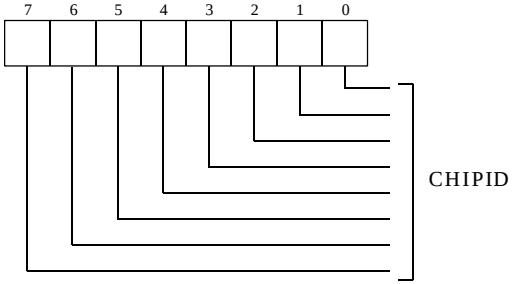
Processor Pins 0=Connected to Vss 1=Open or Pull-UP to Vin					Vcore		Processor Pins 0=Connected to Vss 1=Open or Pull-UP to Vin					Vcore
VID4	VID3	VID2	VID1	VID0	VDC		VID4	VID3	VID2	VID1	VID0	VDC
0	0	0	0	0	2.05		1	0	0	0	0	3.5
0	0	0	0	1	2.00		1	0	0	0	1	3.4
0	0	0	1	0	1.95		1	0	0	1	0	3.3
0	0	0	1	1	1.90		1	0	0	1	1	3.2
0	0	1	0	0	1.85		1	0	1	0	0	3.1
0	0	1	0	1	1.80		1	0	1	0	1	3.0
0	0	1	1	0	-		1	0	1	1	0	2.9
0	0	1	1	1	-		1	0	1	1	1	2.8
0	1	0	0	0	-		1	1	0	0	0	2.7
0	1	0	0	1	-		1	1	0	0	1	2.6
0	1	0	1	0	-		1	1	0	1	0	2.5
0	1	0	1	1	-		1	1	0	1	1	2.4
0	1	1	0	0	-		1	1	1	0	0	2.3
0	1	1	0	1	-		1	1	1	0	1	2.2
0	1	1	1	0	-		1	1	1	1	0	2.1
0	1	1	1	1	-		1	1	1	1	1	-

50-5Fh Bank Select Register(4Eh)



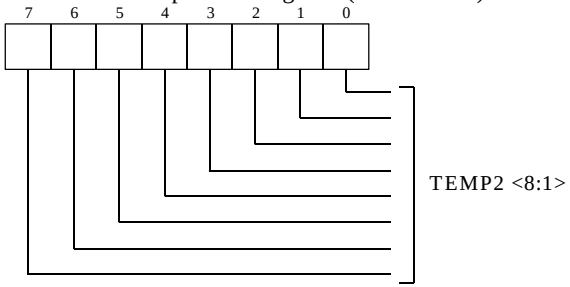
Bit 7:Byte access select for 4Fh (not in use)
Bit 6-3:Reserved
Bit 2-0:Index ports 50h-5Fh Bank Select

Chip ID Register(BANK0:58h)



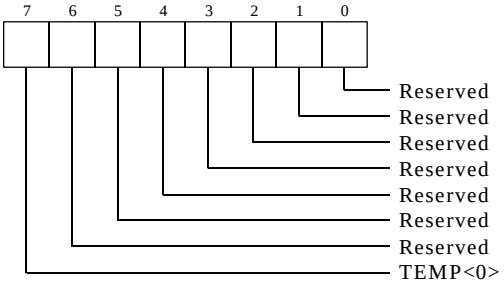
Bit 7-0:Winbond Chip ID number.
Read this register return “11h”.

Temperature Sensor2 Temperature Register1(BANK1:50h)



Please refer to temperature Sensor2 Data Format Table

Temperature Sensor2 Temperature Register2(BANK1:51h)



Please refer to temperature Sensor2 Data Format Table

Temperature Sensor2 Data Format Table:

Temperature	TEMP<8:1>	TEMP<0>
+125ºC	7Dh	0
:	:	:
+25ºC	19h	0
:	:	:
+1ºC	01h	0
+0.5ºC	00h	1
+0ºC	00h	0
-0.5ºC	FFh	1
-1ºC	FFh	0
:	:	:
-25ºC	E7h	0
:	:	:
-55ºC	C9h	0

Chapter 6 BIOS Setup

6.1. Introduction

This chapter discusses Award's Setup program built into the FLASH ROM BIOS. The Setup program allows users to modify the basic system configuration. This special information is then stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

The rest of this chapter is intended to guide you through the process of configuring your system using Setup.

Starting Setup

The Award BIOS is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

1. By pressing <Del> immediately after switching the system on, or
2. By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self-Test).

Press DEL to enter SETUP.

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to...

Press F1 to continue, DEL to enter SETUP

Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Key	Function
Up Arrow	Move to the previous item
Down Arrow	Move to the next item
Left Arrow	Move to the item on the left (menu bar)
Right Arrow	Move to the item on the right (menu bar)
Esc	Main Menu: Quit without saving changes Submenus: Exit Current page to the next higher level menu
Move Enter	Move to the item you desired
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1 key	General help on Setup navigation keys
F5 key	Load previous values from CMOS
F6 key	Load BIOS defaults from BIOS default table
F7 key	Load SETUP defaults
F10 key	Save all the CMOS changes and exit

Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

In Case of Problems

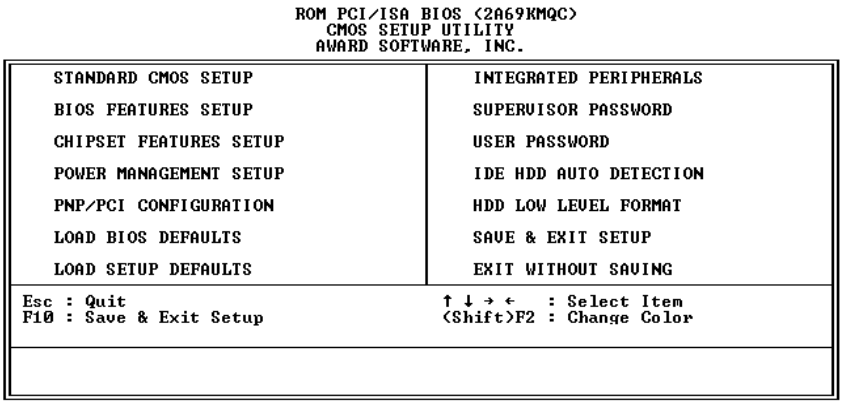
If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings, which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

A Final Note about Setup

The information in this BIOS is subject to change without notice.

6.2. Main Menu



Once you enter the Award BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.

Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

Standard CMOS Features

Use this menu for basic system configuration. See Section 6.3. for the details.

BIOS Features Setup

Use this menu to set the Advanced Features available on your system. See Section 6.4. for the details.

Chipset Features Setup

Use this menu to change the values in the chipset registers and optimize your system's performance. See section 6.5. for the details.

Power Management Setup

Use this menu to specify your settings for power management. See section 6.6. for the details.

PnP / PCI Configuration

This entry appears if your system supports PnP / PCI. See section 6.7. for the details.

Load BIOS Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate. See section 6.8. for the details.

Load SETUP Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs. See section 6.8. for the details.

Integrated Peripherals

Use this menu to specify your settings for integrated peripherals. See section 6.7. for the details.

Supervisor / User Password

Use this menu to set User and Supervisor Passwords. See section 6.10. for the details.

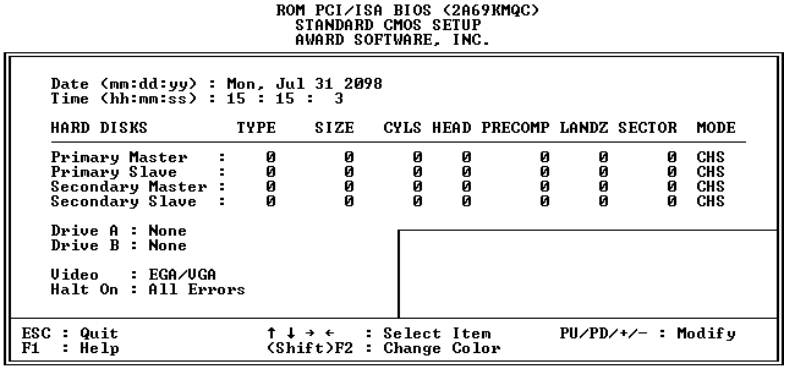
Save & Exit Setup

Save CMOS value changes to CMOS and exit setup. See section 6.11. for the details.

Exit Without Save

Abandon all CMOS value changes and exit setup. See section 6.11. for the details.

6.3. Standard CMOS Setup


ROM PCI/ISA BIOS (2A69KMQC)
STANDARD CMOS SETUP
AWARD SOFTWARE, INC.
Date (mm:dd:yy) : Mon, Jul 31 2098
Time (hh:mm:ss) : 15 : 15 : 3
HARD DISKS TYPE SIZE CYLS HEAD PRECOMP LANDZ SECTOR MODE
Primary Master : 0 0 0 0 0 0 0 CHS
Primary Slave : 0 0 0 0 0 0 0 CHS
Secondary Master : 0 0 0 0 0 0 0 CHS
Secondary Slave : 0 0 0 0 0 0 0 CHS
Drive A : None
Drive B : None
Video : EGA/VGA
Halt On : All Errors
ESC : Quit
F1 : Help
↑ ↓ → ← : Select Item
(Shift)F2 : Change Color
PU/PD/+/- : Modify

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item. Main Menu Selections

This table shows the selections that you can make on the Main Menu

Item	Options	Description
Date	mm dd yy	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	hh : mm : ss	Set the system time
IDE Primary Master	Options are in its sub menu(described in Table 64)	Press <Enter> to enter the sub menu of detailed options
IDE Primary Slave	Options are in its sub menu(described in Table 64)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu(described in Table 64)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu(described in Table 64)	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device

Item	Options	Description
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

IDE Adapters

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive.

Use the legend keys to navigate through this menu and exit to the main menu. Use Table 3 to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
Access Mode	Normal LBA Large Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

6.4. BIOS Features Setup

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

```
                    ROM PCI/ISA BIOS
                  BIOS FEATURES SETUP
                  AWARD SOFTWARE, INC.

Virus Warning                : Enabled     Video  BIOS Shadow  : Disabled
CPU Internal Cache           : Disabled    C8000-CBFFF Shadow  : Disabled
External Cache               : Disabled    CC000-CFFFF Shadow  : Disabled
CPU L2 Cache ECC Checking    : Enabled     D0000-D3FFF Shadow  : Disabled
                                           D4000-D7FFF Shadow  : Disabled
Quick Power On Self Test     : Disabled    D8000-DBFFF Shadow  : Disabled
Boot Sequence                : A,C,SCSI    DC000-DFFFF Shadow  : Disabled
Swap Floppy Drive            : Disabled
Boot Up Floppy Seek          : Disabled
Boot Up NumLock Status       : Off
Gate A20 Option              : Normal
Typematic Rate Setting       : Disabled
Typematic Rate (Chars/Sec)   : 6
Typematic Delay (Msec)       : 250
Security Option              : Setup
PCI/VGA Palette Snoop        : Disabled    ESC : Quit        ↑↓→← : Select Item
Assign IRQ For VGA           : Disabled    F1  : Help        PU/PD/+/- : Modify
OS Select For DRAM > 64MB    : Non-OS2     F5  : Old Values  (Shift)F2 : Color
HDD S.M.A.R.T. capability    : Disabled    F6  : Load BIOS  Defaults
Report No FDD For WIN 95     : No          F7  : Load Setup Defaults
```

Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempts to write data into this area, BIOS will show a warning message on screen and alarm beep.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

CPU Internal Cache/External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design.

Enabled	Enable cache
Disabled	Disable cache

CPU L2 Cache ECC Checking

This item allows you to enable/disable CPU L2 Cache ECC checking.

The choice: Enabled, Disabled.

Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

Boot Sequence

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

The Choice: Floppy, LS/ZIP, HDD, SCSI, CDROM, Disabled.

Swap Floppy Drive

If the system has two floppy drives, you can swap the logical drive name assignments.

The choice: Enabled, Disabled.

Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling speeds boot up.

The choice: Enabled, Disabled.

Boot Up NumLock Status

Select power on state for NumLock.

The choice: Enabled, Disabled.

Gate A20 Option

This entry allows you to select how the gate A20 is handled. The gate A20 is a device used to address memory above 1Mbytes. Initially, the gate A20 was handled via a pin on the keyboard. Today, while keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

The choice: Normal, Fast.

Typematic Rate Setting

Keystroke repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled, Disabled.

Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a keystroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24, 30.

Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750, 1000.

Security Option

Select whether the password is required every time the system boots or only when you enter setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: *To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.*

PCI/VGA Palette Snoop

Some display cards that are non-standard VGA may not show colors properly. This field allows you to set whether MPEG ISA/VESA VGA Cards can work with PCI/VGA or not. When this field is enabled, a PCI/VGA can work with a MPEG ISA/VESA VGA Cards. When this field is disabled, a PCI/VGA cannot work with a MPEG ISA/VESA VGA Cards.

OS Select For DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

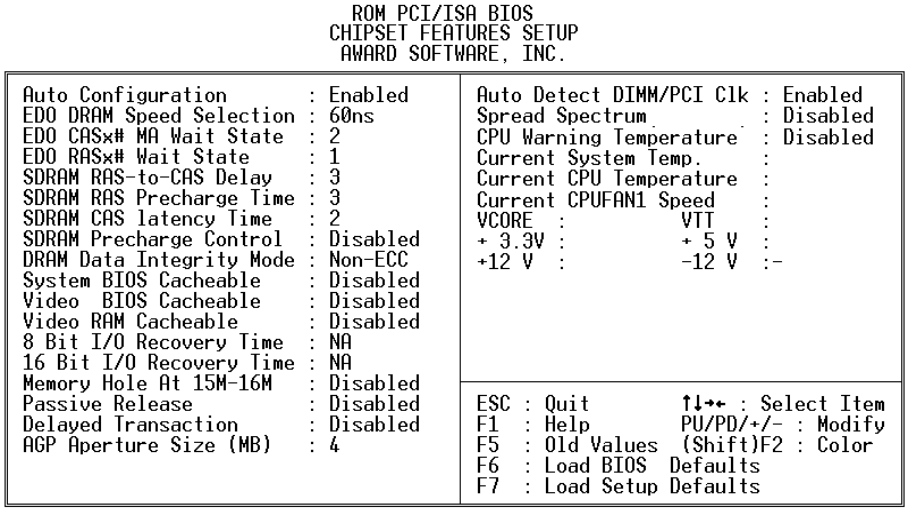
The choice: Non-OS2, OS2.

Report No FDD For Win 95

Whether report no FDD for Win 95 or not.

The choice: Yes, No.

6.5. Chipset Features Setup


ROM PCI/ISA BIOS
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.
Auto Configuration : Enabled
EDO DRAM Speed Selection : 60ns
EDO CASx# MA Wait State : 2
EDO RASx# Wait State : 1
SDRAM RAS-to-CAS Delay : 3
SDRAM RAS Precharge Time : 3
SDRAM CAS latency Time : 2
SDRAM Precharge Control : Disabled
DRAM Data Integrity Mode : Non-ECC
System BIOS Cacheable : Disabled
Video BIOS Cacheable : Disabled
Video RAM Cacheable : Disabled
8 Bit I/O Recovery Time : NA
16 Bit I/O Recovery Time : NA
Memory Hole At 15M-16M : Disabled
Passive Release : Disabled
Delayed Transaction : Disabled
AGP Aperture Size (MB) : 4
Auto Detect DIMM/PCI Clk : Enabled
Spread Spectrum : Disabled
CPU Warning Temperature : Disabled
Current System Temp. :
Current CPU Temperature :
Current CPUFAN1 Speed :
VCORE : VTT :
+ 3.3V : + 5 V :
+12 V : -12 V :-
ESC : Quit ↑↓→← : Select Item
F1 : Help PU/PD/+/- : Modify
F5 : Old Values (Shift)F2 : Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

DRAM Settings

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occurs if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

SDRAM CAS Latency Time

You can select CAS latency time in HCLK of 2/2 or 3/3. The system board designer should set the values in this field, depends on the DRAM installed specifications of the installed DRAM or the installed CPU.

The Choice: 2, 3

DRAM Data Integrity Mode

Select Parity or ECC (error-correcting code), according to the type of installed DRAM.

The Choice: Non-ECC, ECC.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

The choice: Enabled, Disabled.

Video BIOS Cacheable

Select Enabled allows caching of the video BIOS, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

The Choice: Enabled, Disabled.

Video RAM Cacheable

Select Enabled allows caching of the video RAM, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

8 Bit I/O Recovery Time

The recovery time is the length of time, measured in CPU clocks, which the system will delay after the completion of an input/output request. This delay takes place because the CPU is operating so much faster than the input/output bus that the CPU must be delayed to allow for the completion of the I/O.

This item allows you to determine the recovery time allowed for 8 bit I/O.

Choices are from N/A, 1 to 8 CPU clocks.

16 Bit I/O Recovery Time

This item allows you to determine the recovery time allowed for 16 bit I/O.

Choices are from N/A, 1 to 4 CPU clocks.

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA board. This memory must be mapped into the memory space below 16MB.

The Choice: Enabled: Memory hole supported, Disabled: Memory hole not supported.

Passive Release

When Enabled, CPU to PCI bus accesses is allowed during passive release. Otherwise, the arbiter only accepts another PCI master access to local DRAM.

The choice: Enabled, Disabled.

Delay Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

The Choice: Enabled, Disabled.

AGP Aperture Size (MB)

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded. Host cycles that hit the aperture range are forwarded to the AGP without any translation.

The Choice: 4, 8, 16, 32, 64, 128, 256

Auto Detect DIMM/PCI CLK

This item allows you to enable/disable auto detect DIMM/PCI Clock.

The choice: Enabled, Disabled.

Spread Spectrum

This item allows you to enable/disable the spread spectrum modulate.

The choice: Enabled, Disabled.

CPU Warning Temperature

This item allows you to enable/disable the CPU warning temperature, if your computer contains a monitoring system.

The choice: Enabled, Disabled.

Current System Temp

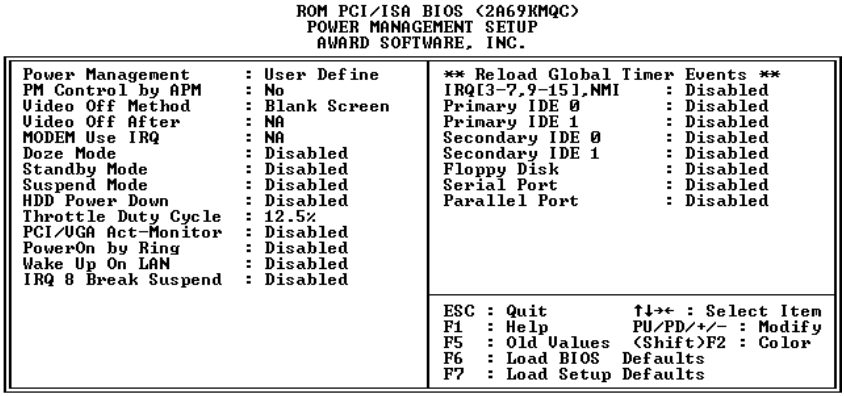
This field displays the Current system temperature, if your computer contains a monitoring system.

Current CPUFAN1 Speed

This field displays the current speed of CPU fan, if your computer contains a monitoring system.

6.6. Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.


ROM PCI/ISA BIOS (2A69KMQC)
POWER MANAGEMENT SETUP
AWARD SOFTWARE, INC.
Power Management : User Define
PM Control by APM : No
Video Off Method : Blank Screen
Video Off After : NA
MODEM Use IRQ : NA
Doze Mode : Disabled
Standby Mode : Disabled
Suspend Mode : Disabled
HDD Power Down : Disabled
Throttle Duty Cycle : 12.5%
PCI/VGA Act-Monitor : Disabled
PowerOn by Ring : Disabled
Wake Up On LAN : Disabled
IRQ 8 Break Suspend : Disabled
** Reload Global Timer Events **
IRQ[3-7,9-15],NMI : Disabled
Primary IDE 0 : Disabled
Primary IDE 1 : Disabled
Secondary IDE 0 : Disabled
Secondary IDE 1 : Disabled
Floppy Disk : Disabled
Serial Port : Disabled
Parallel Port : Disabled
ESC : Quit ↑↓→← : Select Item
F1 : Help PU/PD/+/- : Modify
F5 : Old Values (Shift)F2 : Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

Power Management

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

1. HDD Power Down
2. Doze Mode
3. Suspend Mode
4. Standby Mode

There are four selections for Power Management, three of which have fixed mode settings.

Disable (default)	No power management. Disables all four modes
Min. Power Saving	Minimum power management. Doze Mode = 1 hr. Standby Mode = 1 hr., Suspend Mode = 1 hr., and HDD Power Down = 15 min.
Max. Power Saving	Maximum power management -- **ONLY AVAILABLE FOR SL CPU's**. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min., and HDD Power Down = 1 min.
User Define	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

PM Control by APM

When enabled, an Advanced Power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock.

If the Max. Power Saving is not enabled, this will be preset to No.

Video Off Method

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank	This selection will cause the system to turn off the vertical and horizontal synchronization ports and writes blanks to the video buffer.
Blank Screen	This option only writes blanks to the video buffer.
DPMS	Initial display power management signaling.

Video Off After

When enabled, this feature allows the VGA adapter to operate in a power saving mode.

N/A	Monitor will remain on during power saving mode.
Suspend	Monitor blanked when the system enters the Suspend mode.
Standby	Monitor blanked when the system enters the Standby mode.
Dose	Monitor blanked when the system enters any power saving mode.

MODEM Use IRQ

Name the interrupt request (IRQ) line assigned to modem (if any) on your system. Activity of the selected IRQ always awakens the system.

The choice: NA, 3, 4, 5, 7, 9, 10, 11.

PM Timers

The following four modes are Green PC power saving functions which are only user configurable when *User Defined* Power Management has been selected. See above for available selections.

Doze Mode

When enabled and after the set time of system inactivity, the CPU clock will run at slower speed while all other devices still operate at full speed.

Standby Mode

When enabled and after the set time of system inactivity, the fixed disk drive and the video would be shut off while all other devices still operate at full speed.

Suspend Mode

When enabled and after the set time of system inactivity, all devices except the CPU will be shut off.

HDD Power Down

When enabled and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active.

Throttle Duty Cycle

When the system enters Doze mode, the CPU clock runs only part of the time that the clock runs.

The choice: 12.5%, 25.0%, 37.5%, 50.0%, 62.5%, 75.0%

PCI/VGA Act-Monitor

When enabled, any video activity restarts the global timer for Standby mode.

The choice: Enabled, Disabled

Power On by Ring

An input signal on the serial Ring Indicator (RI) line (an incoming call on the modem) awakens the system.

Wake Up On LAN

This does not support Wake On LAN, so it is impossible to change setting.

IRQ 8 Break Suspend

You can enabled or disable monitoring of IRQ8 so it does not awaken the system from Suspend mode.

The choice: Enabled, Disabled.

Reload Global Timer Event

When enabled, an event occurring on each device listed below restarts the global time for Standby mode.

IRQ (3 – 7, 9 – 15), NMI

Primary IDE 0

Primary IDE 1

Secondary IDE 0

Secondary IDE 1

FDD, COM, LPT Port

PCI PIRQ[A-D] #

6.7. PnP/PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

```
ROM PCI/ISA BIOS (2A69KMQC)
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC.

PNP OS Installed          : No          Used MEM base addr  : D000
Resources Controlled By   : Manual      Used MEM Length     : 8K
Reset Configuration Data  : Enabled     Assign IRQ For USB  : Enabled

IRQ-3  assigned to : PCI/ISA PnP
IRQ-4  assigned to : PCI/ISA PnP
IRQ-5  assigned to : PCI/ISA PnP
IRQ-7  assigned to : PCI/ISA PnP
IRQ-9  assigned to : PCI/ISA PnP
IRQ-10 assigned to : PCI/ISA PnP
IRQ-11 assigned to : PCI/ISA PnP
IRQ-12 assigned to : PCI/ISA PnP
IRQ-14 assigned to : PCI/ISA PnP
IRQ-15 assigned to : PCI/ISA PnP
DMA-0  assigned to : PCI/ISA PnP
DMA-1  assigned to : PCI/ISA PnP    ESC : Quit         ↑↓→← : Select Item
DMA-3  assigned to : PCI/ISA PnP    F1  : Help         PU/PD/+/- : Modify
DMA-5  assigned to : PCI/ISA PnP    F5  : Old Values   (Shift)F2 : Color
DMA-6  assigned to : PCI/ISA PnP    F6  : Load BIOS  Defaults
DMA-7  assigned to : PCI/ISA PnP    F7  : Load Setup Defaults
```

PNP OS Installed

Select Yes if the system-operating environment is Plug-and-Play aware (e.g. Windows 95).

The choice: Yes, No.

Resource Controlled by

The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play – compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

The choice: Auto and Manual.

Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system can not boot.

The choice: Enabled, Disabled.

IRQ n Assigned to

When resources are controlled manually, assign each system interrupt as on of the following type, depending on the type of device using the interrupt.

Legacy ISA Devices compliant with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ4 for serial port 1)

PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

The Choice: *Legacy ISA* and *PCI/ISA PnP*.

DMA n Assigned to

When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt:

Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

Choices are *Legacy ISA* and *PCI/ISA PnP*.

PCI IDE IRQ Map to

This field lets you select PCI IDE IQR mapping or PC AT (ISA) interrupts. If your system does not have one or two PCI IDE connectors on the system board, select values according to the type of IDE interface(s) installed in your system (PCI or ISA). Standard ISA interrupts for IDE channels are IRQ14 for primary and IRQ15 for Secondary.

The choice: PCI-SLOT1, PCI-SLOT2, PCI-SLOT3, PCI-SLOT4, ISA, PCI-AUTO

Primary / Secondary IDE INT#

Each PCI peripheral connection is capable of activating up to four interrupts: INTA#, INTB#, INTC#, INTD#. By default, a PCI connection is assigned INTA#. Assigning INTB# has no meaning unless the peripheral device requires two interrupt services rather than just one. Because the PCI IDE interface in the chipset has two channels, it requires two interrupt services. The primary and secondary IDE INT# fields default to values appropriate for two PCI IDE channels, with the primary PCI IDE channel having a lower interrupt than the secondary.

Used MEM base addr

Select a base address for the memory area used by any peripheral that requires high memory.

The Choice: C800, CC00, D000, D400, D800, DC00, N/A.

Used MEM Length

Select a length for the memory area specified in the previous field. This field does not appear if no base address is specified.

The choice: 8K, 16K, 32K, 64K.

6.8. Defaults Menu

Selecting “Defaults” from the main menu shows you two options, which are described below.

Load BIOS Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Load BIOS Defaults (Y/N) ? N

Pressing ‘Y’ loads the BIOS default values for the most stable, minimal-performance system operations.

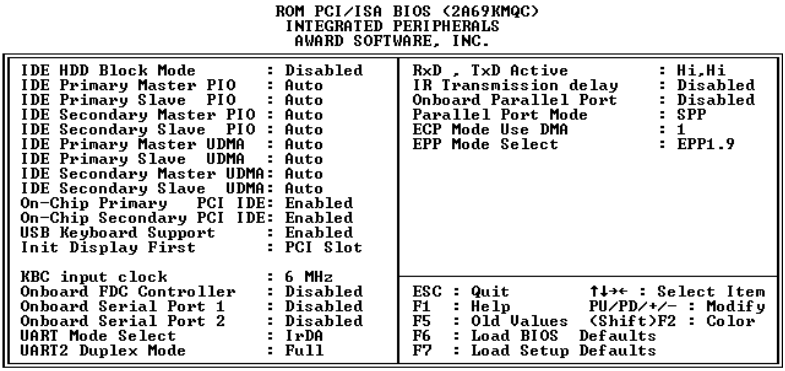
Load SETUP Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Load SETUP Defaults (Y/N) ? N

Pressing ‘Y’ loads the default values that are factory settings for optimal performance system operations.

6.9. Integrated Peripherals


ROM PCI/ISA BIOS (2A69KMQC)
INTEGRATED PERIPHERALS
AWARD SOFTWARE, INC.
IDE HDD Block Mode : Disabled
IDE Primary Master PIO : Auto
IDE Primary Slave PIO : Auto
IDE Secondary Master PIO : Auto
IDE Secondary Slave PIO : Auto
IDE Primary Master UDMA : Auto
IDE Primary Slave UDMA : Auto
IDE Secondary Master UDMA: Auto
IDE Secondary Slave UDMA: Auto
On-Chip Primary PCI IDE: Enabled
On-Chip Secondary PCI IDE: Enabled
USB Keyboard Support : Enabled
Init Display First : PCI Slot
KBC input clock : 6 MHz
Onboard FDC Controller : Disabled
Onboard Serial Port 1 : Disabled
Onboard Serial Port 2 : Disabled
UART Mode Select : IrDA
UART2 Duplex Mode : Full
RxD , TxD Active : Hi,Hi
IR Transmission delay : Disabled
Onboard Parallel Port : Disabled
Parallel Port Mode : SPP
ECP Mode Use DMA : 1
EPP Mode Select : EPP1.9
ESC : Quit ↑↓→← : Select Item
F1 : Help PU/PD/+/- : Modify
F5 : Old Values (Shift)F2 : Color
F6 : Load BIOS Defaults
F7 : Load Setup Defaults

IDE HDD Block Mode

This allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive (HDD)

The choice: Enabled, Disabled.

IDE Primary/Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

The choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, Mode 4.

IDE Primary/Secondary Master/Slave UDMA

Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.

The Choice: Auto, Disabled.

On-Chip Primary/Secondary PCI IDE

The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select *Enabled* to activate each channel separately.

The choice: Enabled, Disabled.

USB Keyboard Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

The choice: Enabled, Disabled.

Init Display First

It is impossible to change the setting.

Onboard FDC Controller

Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field.

The choice: Enabled, Disabled.

Onboard Serial Port 1/Port 2

Select an address and corresponding interrupt for the first and second serial ports.

The choice: 3F8/IRQ4, 2E8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto.

UART Mode Select

This item allows you to determine which Infra Red IR) function of onboard I/O chip.

The Choice: Normal ASKIR, IrDA

UART 2 Duplex Select

Select the value required by the IR device connected to the IR port. Full-duplex mode permits transmission in one direction only at a time.

The Choice: Half, Full

RxD, TxD Active

This item allows you to determine the active of RxD, TxD.

The Choice: “Hi, Hi”, “Lo, Lo”, ”Lo, Hi”, ”Hi, Lo”

Onboard Parallel Port

Select a logical LPT port name and matching address for the physical parallel (printer) port.

The Choice: 378H/IRQ7, 278H/IRQ5, 3BCH/IRQ7, Disabled

Parallel Port Mode

Selected an operating mode for the onboard parallel port. Select Compatible or extended unless you are certain both your hardware and software support EPP or ECP mode.

The Choice: SOOM ECO + EPP1.7, EPP 1.7+SPP, EPP 1.9+SPP; ECP, ECP + EPP 1.9 and Normal.

ECP Mode Use DMA

Select a DMA channel for the port.

The Choice are 3, 1

6.10. Supervisor/User Password Setting

You can set either supervisor or user password, or both of then. The differences between are:

SUPERVISOR PASSWORD: can enter and change the options of the setup menus.

USER PASSWORD: just can only enter but do not have the right to change the options of the setup menus. When you select this unction, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD: Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED: When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup.

> ***Note:*** *Once you register the Password, you can't cancel the Password function if you don't have the Password. Please be careful to treat the password.*

6.11. Exit Selecting

Save & Exit Setup

Pressing <Enter> on this item asks for confirmation:

Save to CMOS and EXIT (Y/N)? Y

Pressing "Y" stores the selections made in the menus in CMOS – a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Exit Without Saving

Pressing <Enter> on this item asks for confirmation:

Quit without saving (Y/N)? Y

This allows you to exit Setup without storing in CMOS any change. The previous selections remain in effect. This exits the Setup utility and restarts your computer.

6.12. POST Messages

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

6.13. POST Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

6.14. Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

CMOS battery has failed

CMOS battery is no longer functional. It should be replaced.

CMOS checksum error

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT failure

INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette drives or types mismatch error

RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

Display switch is set incorrectly

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

Display type has changed since last BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

EISA configuration checksum error

PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the board is installed firmly in the slot.

EISA configuration is not complete

PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

> ***Note:*** *When either of these errors appear, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.*

Error encountered initializing hard drive

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

Error initializing hard disk controller

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy disk controller error or no controller present

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

Invalid EISA configuration

PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

> ***NOTE:*** *When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.*

Keyboard error or no keyboard present

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

Memory address error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory parity error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory size has changed since last BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

Memory verify error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending address not found

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

Offending segment

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

Press a key to REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

Press F1 to disable NMI, F2 to REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM parity error

CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

Should be empty but EISA board found

PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

> ***NOTE****: When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.*

Should have EISA board but not found

PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

> ***NOTE:*** *When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.*

Slot not empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

> ***NOTE:*** *When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.*

System halted, (CTRL-ALT-DEL) to REBOOT ...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Wrong board in slot

PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

> ***NOTE:*** *When this error appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.*

Floppy disk(s) fail (80)

Unable to reset floppy subsystem.

Floppy disk(s) fail (40)

Floppy Type dismatch.

Hard disk(s) fail (80)

HDD reset failed.

Hard disk(s) fail (40)

HDD controller diagnostics failed.

Hard disk(s) fail (20)

HDD initialization error.

Hard disk(s) fail (10)

Unable to recalibrate fixed disk.

Hard disk(s) fail (08)

Sector Verify failed.

Keyboard is locked out - Unlock the key.

Unlock the key. BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

Keyboard error or no keyboard present

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

Manufacturing POST loop

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

BIOS ROM checksum error - System halted

The checksum of ROM address F0000H-FFFFFH is bad.

Memory test fail

BIOS reports the memory test fail if the onboard memory is tested error.

6.15. POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved

POST (hex)	Description
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel®) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved

POST (hex)	Description
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0~640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved

POST (hex)	Description
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved

POST (hex)	Description
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved

POST (hex)	Description
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved

POST (hex)	Description
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ◆Clear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code

POST (hex)	Description
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)

A-46-427
LZS2451
021030 [010606]